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10/567,241	01/04/2007	Takuji Maeda	0074/065001	9459

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EXAMINER	
BERTRAM, RYAN	
ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,241	MAEDA ET AL.	
	Examiner	Art Unit	
	RYAN BERTRAM	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/6/2006* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/6/2006, 7/9/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/567,241 has a total of 27 claims pending in the application, there are 3 independent claims and 24 dependent claims, all of which are ready for examination by the examiner.

I. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 14, and 16-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Sasaki (US 2005/0080985).

1. Regarding claim 1, Sasaki discloses a semiconductor memory card which is used in connecting to an access device, comprising:

a host interface which transmits a control signal and data to the access device and receives a signal from the access device **[see Fig. 4, interface on left provides communication between access device and memory]**;

a nonvolatile memory in which a plurality of continuous sectors are grouped into an erase block as a minimum unit for data erasing and which includes an address management information area and user data area **[see Fig. 4, element 17 & paragraph 73; memory divided into erase blocks]**;

a memory controller which controls erasing, writing and reading of data for said nonvolatile memory **[see Fig. 4, element 16; controller]**;

a memory for card information storage including a card information storage part which stores information on access condition as condition at least at the time when said access device accesses said semiconductor memory card and access performance which said semiconductor memory card realizes when said access device performs access on said access condition **[see paragraph 83; memory card stores system information storage size and device type]**, and

a control part which controls each part on the basis of the control signal acquired via said interface **[see paragraph 89; memory card is controlled based on attributes read out]**.

2. Regarding claim 2, Sasaki discloses the semiconductor memory card according to claim 1, wherein said card information storage part stores

first information on physical characteristics of in said semiconductor memory card **[see paragraph 83; flash memory model number, etc]**, and at least one of

second information on access condition **[see paragraph 83; read/write feasibility, read-only, etc]**

third information on said access rate of said semiconductor memory card as information on said access performance, and

fourth information on abnormal process of said semiconductor memory card.

3. Regarding claim 14, Sasaki discloses the semiconductor memory card according to claim 1, wherein said card information storage part has an access performance basic information list which holds various process time and process unit size in said semiconductor memory card according to an access method, and in response to a request from said access device, said control part transmits said access performance basic information list to said access device **[see paragraph 87; number of bytes per sector]**.

4. Regarding claim 16, Sasaki discloses an access device for accessing a semiconductor memory card in which a plurality of continuous sectors are grouped into a block as a minimum unit for data erasing and stored data is managed according to a file system comprising:

a card information acquisition part for acquiring information on access condition as condition at the time when said access device accesses said semiconductor memory card and access performance which said semiconductor memory card realizes when said access device performs access on said access condition from said semiconductor memory card **[see paragraph 89; memory card attributes acquired from memory]**;

a card use condition storage part for storing information on access condition which can be used when said access device accesses said semiconductor memory card and information on access rate desirable for said semiconductor memory card **[see paragraph 83; memory card stores system information storage size and device type]**;

an access condition determination part for determining access condition on the basis of the information acquired by said card information acquisition part, information on access performance of said semiconductor memory card and information stored in said card use condition storage part **[see paragraph 89; memory card attributes acquired from memory]**;

a file system control part for acquiring access condition determined by said access condition determination part and performing file access suitable for said access condition **[see paragraph 89; memory card attributes acquired from memory]**; and

an access control part for accessing said semiconductor memory card in response to an access request from said file system control part **[see paragraph 55; controller controls access to memory device]**.

5. Regarding claim 17, Sasaki discloses the access device according to claim 16, wherein said access condition determination part divides an area of said semiconductor memory card in file system access units (hereinafter referred to as FS access unit) on the basis of the information on access performance acquired from said semiconductor memory card **[see paragraphs 63 & 87; unit size is stored based on file system]**.

6. Regarding claim 18, Sasaki discloses the access device according to claim 17, wherein said file system control part, when recording file data on said semiconductor memory card, determines a continuous free area having a length of multiples of said FS access unit on the basis of management information of a file system constructed on said semiconductor memory card, and records the file data in said determined continuous free area **[see paragraphs 72-73; data stored in blocks of user area]**.

7. Regarding claim 19, Sasaki discloses the access device according to claim 17, wherein said file system control part, when recording new file management information on said semiconductor memory card, determines whether or not another file management information is recorded in the area of said FS access unit on the basis of management information of the file system constructed on said semiconductor memory card and a free area for writing new file management information therein exists, and when the free area exists, determines said free area as a writing position of file management information, and records the file management information in said determined free area **[see paragraph 72; memory device divided into user area and system area]**.

8. Regarding claim 20, Sasaki discloses the access device according to claim 17, wherein said file system control part, when the areas of a plurality of said FS access units are partially used, moves data in the used areas of partially used FS access units

to an unused area of the other FS access unit on the basis of management information of a file system constructed on said semiconductor memory card **[see paragraphs 74-75; used blocks and spare blocks are managed]**.

9. Regarding claim 21, Sasaki discloses the access device according to claim 17, wherein said file system control part calculates the number of areas in which the whole of said FS access unit is the free area on the basis of management information of the file system constructed on said semiconductor memory card **[see paragraph 76; spare blocks are managed on the memory device]**.

10. Regarding claim 22, Sasaki discloses an access method for accessing a semiconductor memory card in which a plurality of continuous sectors are grouped into a block as a minimum unit for data erasing and stored data is managed according to the file system comprising:

a card use condition storage step for storing information on access condition which can be used when accessing said semiconductor memory card and information on access rate desirable for said semiconductor memory card **[see paragraph 83; system information recorded on memory card]**;

a card information acquisition step for acquiring information on access on access condition as condition at the time when said access device accesses said semiconductor memory card and access performance which said semiconductor memory card realizes when said access device performs access on said access

condition from said semiconductor memory card **[see paragraph 114; attributes are read from memory device]**;

an access condition determination step for determining access condition on the basis of the information acquired in said card information acquisition step and information stored in said card use condition storage step **[see paragraph 114; attributes are read from memory device]**; and

a file system control step for acquiring access condition determined in said access condition determination step and accessing a file in said semiconductor memory card so as to meet said access condition **[see paragraph 89; memory card is controlled based on attributes read out]**.

11. Regarding claim 23, Sasaki discloses the access method according to claim 22, wherein said access condition determination step determines a file system access unit (hereinafter referred to as FS access unit) as a size used when accessing said semiconductor memory card according to said access condition **[see paragraphs 63 & 87; unit size is stored based on file system]**.

12. Regarding claim 24, Sasaki discloses the access method according to claim 23, wherein when recording file data on said semiconductor memory card, said file system control step determines a continuous free area having a length of multiples of said FS access unit on the basis of management information of the file system constructed on

said semiconductor memory card, and the file data is recorded in said determined continuous free area **[see paragraphs 72-73; data stored in blocks of user area]**.

13. Regarding claim 25, Sasaki discloses the access method according to claim 23, wherein when recording new file management information on said semiconductor memory card, said file system control step determines whether or not another file management information is recorded in the area of said FS access unit on the basis of management information of the file system constructed on said semiconductor memory card and a free area for writing new file management information therein exists, and when the free area exists, said space area is determined as a writing position of file management information and records the file management information in said determined free area **[see paragraph 72; memory device divided into user area and system area]**.

14. Regarding claim 26, Sasaki discloses the access method according to claim 23, wherein when the areas of a plurality of said FS access units are partially used, said file system control step moves data in the used areas of partially used FS access units to an unused area of the other FS access unit on the basis of management information of the file system constructed on said semiconductor memory card **[see paragraphs 74-75; used blocks and spare blocks are managed]**.

15. Regarding claim 27, Sasaki discloses the access method according to claim 23, wherein said file system control step calculates the size of an area in which the whole of said access unit is a free area on the basis of management information of the file system constructed on said semiconductor memory card, and the calculated value is informed as a free area length of said semiconductor memory card to an application program **[see paragraph 76; spare blocks are managed on the memory device]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Hayashi et al. (US 5,434,618).

16. Regarding claim 3, Sasaki discloses the semiconductor memory card according to claim 2 as described above.

Sasaki does not expressly disclose that the third information includes a flag representing rate performance of said semiconductor memory card as said information on access rate.

Hayashi discloses a flash memory controller that contains a register that represents the rate performance of the card **[see Col. 5, lines 30-60]**.

Sasaki and Hayash are analogous art because they are from the same field of endeavor, namely controlling memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art utilize the teachings of Hayashi and store the memory rate performance in the memory card.

The motivation for doing so would have been to make the most of the characteristics of the card **[see Hayashi, Col. 7, lines 25-28]**.

Therefore, it would have been obvious to combine Sasaki with Hayashi for the benefit of making the most of the memory's performance characteristics, to obtain the invention as specified in claim 3.

17. Regarding claim 4, Sasaki and Hayashi disclose the semiconductor memory card according to claim 1, wherein said card information storage part stores at least first information on physical characteristics in said semiconductor memory card **[see Sasaki, paragraph 83; flash memory model number, etc]**, second information on said access condition **[see Sasaki, paragraph 83; read/write feasibility, read-only, etc]**, and third information on access rate of said semiconductor memory card as information on said access performance **[see Hayashi, Col. 5, lines 30-60; access rate]**.

18. Regarding claim 5, Sasaki and Hayashi disclose the semiconductor memory card according to claim 4, wherein said control part, in response to a request from said access device, reads information on access condition for accessing said semiconductor memory card, and information on access rate when accessing to said semiconductor memory card on said access condition from said card information storage part, and transmits the information to said access device **[see Hayashi Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

19. Regarding claim 6, Sasaki and Hayashi disclose the semiconductor memory card according to claim 4, wherein said control part, in response to information on access condition designated by said access device, reads information on access rate when accessing the semiconductor memory card on said access condition from said card information storage part, and transmits the information to said access device **[see Hayashi Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

20. Regarding claim 7, Sasaki and Hayashi disclose the semiconductor memory card according to claim 4, wherein said control part, in response to information on access rate designated by said access device, reads information on access condition to said semiconductor memory card required to meet said access rate from said card information storage part, and transmits the information to said access device **[see Hayashi Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

21. Regarding claim 8, Sasaki and Hayashi disclose the semiconductor memory card according to claim 4, wherein said control part, when reading information on access condition designated by said access device and information on access rate from said card information storage part and accessing said semiconductor memory card on said access condition, determines whether or not the access rate is met and transmits a

determination result to said access device **[see Hayashi Col. 6, lines 33-40; access rate read from card by access device and card utilizes rate information]**.

22. Regarding claim 9, Sasaki and Hayashi disclose the semiconductor memory card according to claim 4, wherein the third information in said card information storage part includes a flag representing rate performance of said semiconductor memory card as said information on access rate **[see Hayashi, Col. 5, lines 30-60; access rate information stored in register in memory]**.

23. Regarding claim 15, Sasaki and Hayashi disclose the semiconductor memory card according to claim 1, wherein said card information storage part holds process unit size of said semiconductor memory card, access method and access rate in the case where access condition containing process contents are changed, and in response to request of said access device, said control part transmits information on said access rate to said access device **[see Hayashi Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Hayashi as applied to claim 4 above, and further in view of Koizumi et al. (US 2003/0026030).

24. Regarding claim 10, Sasaki and Hayashi disclose the semiconductor memory card according to claim 4 as described above.

Sasaki and Hayashi do not expressly disclose card information storage part has information on access rate of said semiconductor memory for a plurality of levels of power consumption of said semiconductor memory card as said third information, and said control part.

Koizumi discloses a memory device that stores information on access rate based on various power levels **[see Fig. 3 & paragraph 109]**.

Sasaki, Hayashi, and Koizumi are analogous art because they are from the same field of endeavor, namely controlling access to memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art utilize the teachings of Koizumi and store the access rates based on various power levels of the memory device of Sasaki and Hayashi.

The motivation for doing so would have been to make efficient use of power **[see Koizumi, paragraph 36]**.

Therefore, it would have been obvious to combine Sasaki and Hayashi with Koizumi for the benefit of making efficient use of power, to obtain the invention as specified in claim 10.

25. Regarding claim 11, Sasaki, Hayashi, and Koizumi disclose the semiconductor memory card according to claim 4, wherein said card information storage part has information on access rate of said semiconductor memory for a plurality of levels of power consumption of said semiconductor memory card as said third information, and said control part **[see Koizumi, Fig. 3 & paragraph 109]**, in response to information on access condition designated by said access device and designation of power consumption level, reads information on access rate when accessing said semiconductor memory card on said access condition and designated electrical power consumption level from said card information storage part, and transmits the information to said access device **[see Hayashi Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

26. Regarding claim 12, Sasaki, Hayashi, and Koizumi disclose the semiconductor memory card according to claim 4, wherein said card information storage part has information on access rate of said semiconductor memory for a plurality of levels of power consumption of said semiconductor memory card as said third information, and said control part **[see Koizumi, Fig. 3 & paragraph 109]**, in response to information on access rate designated by said access device and designation of power consumption

level, reads information on access condition to said semiconductor memory card required to meet said access rate from said card information storage part, and transmits the information to said access device **[see Hayashi Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

27. Regarding claim 13, Sasaki, Hayashi, and Koizumi disclose he semiconductor memory card according to claim 4, wherein said card information storage part has information on access rate of said semiconductor memory for a plurality of levels of power consumption of said semiconductor memory card as said third information **[see Koizumi, Fig. 3 & paragraph 109]**, and said control part reads information on access condition designated by said access device and information on designation of power consumption level and access rate from said card information storage part, determines whether or not said access rate is met when accessing said semiconductor memory card on said access condition and designated electrical power level, and transmits a determination result to said access device **[see Hayashi Col. 6, lines 33-40; attributes and access rate read from card by access device]**.

II. CLOSING COMMENTS

Conclusion

(a) **Status of Claims In the Application**

(i) Claims Rejected In the Application

Per the instant office action, claims 1-27 have received a first action on the merits and are subject of a first action non-final.

(b) **Directions of Future Correspondences**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Bertram whose telephone number is 571-270-1377. The examiner can normally be reached on Mon-Fri 8am-5pm ET.

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on 571-272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan Bertram/
Examiner, Art Unit 2187

/Kevin L Ellis/

Acting SPE of Art Unit 2187